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Transmitted herewith for filing is the Patent Application of:

Inventors: Leslie C. Jenkins, Frank R. Libsch, Michael P. Mastro,  
Robert W. Nywening and Robert John Polastre

For: INTEGRATED CIRCUITS FOR A DISPLAY ARRAY

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☒ 12 Sheets of Informal Drawings.

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Respectfully submitted,

By Jay P. Sbrollini  
Attorney: Jay P. Sbrollini  
Registration No.: 36,266  
Tel. (914) 945-2587

IBM CORPORATION  
INTELLECTUAL PROPERTY LAW DEPT.  
P.O. BOX 218  
YORKTOWN HEIGHTS, NY 10598

## **Integrated Circuits for a Display Array**

### **BACKGROUND OF THE INVENTION**

#### *Technical Field*

The invention relates to liquid crystal display (LCD) arrays.

#### *5 Description of the Related Art*

An array tester as described in United States Patent No. 5,179,345 and 5,546,013 provides a means for testing the cells of an TFT/LCD display array by coupling test probes to the gate line pads and data line pads that terminate the gate lines and data lines, respectively, of the TFT/LCD array.

10 Importantly, when the size of the TFT/LCD display array under test is changed, the spacing of the gate lines and/or data lines and the pads terminating thereof change. In order to test such an array, the probe fixture for the gate lines and/or data lines must be redesigned to accommodate for the variation in spacing, which is a costly solution.

In addition, when the resolution of the TFT/LCD display array under test results is  
15 changed, the number of gate lines and/or data lines and pads terminating thereof changes. In order to test such an array, the probe fixture for the gate lines and/or data lines must be redesigned to accommodate for the variation in the number of gate lines and/or data lines. Moreover, the gate line drive circuitry and/or the data line drive/sense circuitry and the control routine must be updated to accommodate for the variation in the number of the gate lines and/or  
20 data lines. Such design modifications are also very costly.

Thus, there remains a need in the art for an array test system whereby the configuration of the array test system can be changed with minimal costs in order to accommodate variations in the size and/or resolution of the TFT/LCD display arrays under test.

In addition, there remains a need in the art for circuitry integrated onto the substrate that enables reconfiguration of the array test system with minimal costs.

## SUMMARY OF THE INVENTION

The problems stated above and the related problems of the prior art are solved with the principles of the present invention, integrated circuits for display arrays. The present invention provides a device for use in a display system comprising an array of pixel cells formed on a substrate. Each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The device comprises first and second transistors formed on said substrate. Each transistor has a gate electrode and first and second electrodes defining a serpentine channel region there between. Voltage applied to the gate electrode controls conductivity of the channel region. Preferably, the a common electrode comprises one of the first and second electrodes of said first transistor and one of said first and second electrodes of said second transistor. The first and second transistors are preferably coupled between a gate line (or data line) and respective probe pads formed on the substrate and selectively couple the respective probe pad to the gate line (or data line) during a test routine whereby charge is written to, stored, and read from the array of pixel cells.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(A) is a pictorial illustration of the display array test system of the present invention.

FIG. 1(B) is a pictorial illustration of an exemplary array of pixel cells and the gate lines and data lines connected thereto.

FIG. 2 is a functional block diagram illustrating the gate line select/hold circuitry of FIG. 1(A) for a group of gate lines.

FIG. 3 is a functional block diagram illustrating the data line select/hold circuitry of FIG. 1(A) for a group of data lines.

5 FIG. 4(A) is a flow chart illustrating the control of the gate line select/hold circuitry and data line select/hold circuitry of FIGS. 2 and 3 in writing charge to a cell connected to an exemplary gate line/data line pair ( $GL_0$ ,  $DL_3$ ) in an addressing cycle.

FIG. 4(B) is a timing diagram of an exemplary implementation of the control of FIG. 4(A).

10 FIG. 5(A) is a flow chart illustrating the control of the gate line select/hold circuitry and data line select/hold circuitry of FIGS. 2 and 3 in reading charge from a cell connected to an exemplary gate line/data line pair ( $GL_0$ ,  $DL_3$ ) in an address cycle.

FIG. 5(B) is a timing diagram of an exemplary implementation of the control of FIG. 5(A).

15 FIG. 6 is a functional block diagram illustrating a preferred embodiment of the gate line drive module of FIG. 1.

FIG. 7 is a functional block diagram illustrating a preferred embodiment of the data line drive/sense module of FIG. 1

20 FIG. 8 is a schematic diagram of a select transistor/hold transistor pair corresponding to single gate line in a group of gate lines according to the present invention.

FIG. 9 is a schematic diagram of a select transistor/hold transistor pair corresponding to single data line in a group of data lines according to the present invention.

FIG. 10(A) illustrates the electrodes of a select/hold transistor pair.

FIG. 10(B) is a top view illustrating the layout of the select/hold transistor pair of FIG.

5 10(A).

FIG. 10(C) represents a cross-section A-A' of an exemplary embodiment of the hold transistor of FIG. 10(B) implemented as a bottom-gate TFT transistor.

## DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 1(A), a substrate 10 having formed thereon an array of TFT/LC pixel cells 12 is supported on a substrate holder 14. Substrate 10 has a number of gate lines 16 and data lines 18 formed thereon that are electrically coupled to the TFTs (not shown) of the cells to drive the array of cells 12. FIG. 1(B) illustrates the array of cells 12 formed on the substrate 10. Each pixel cell 12 includes a TFT 19 coupled to a gate line 16 and data line 18.

The basic routine for testing the array is as follows: biasing the gate line 16 and data line 18 connected to a cell 12 such that the TFT of the cell 12 is in a conductive (ON) state and charge is written to the cell 12, storing the charge in the cell 12 by biasing the gate line 16 and data line 18 connected to the cell 12 such that the TFT of the cell 12 is in a nonconductive (OFF) state, and reading the charge stored in the cell 12. Reading the charge stored in a cell 12 is accomplished by electrically coupling sense circuitry to the data line 18 connected to the cell 12 and biasing the gate line 16 connected to the cell 12 such that TFT 19 of the cell is in a conductive (ON) state, thereby allowing the charge stored in the cell 12 to be transferred to sense circuitry. The charge transferred to the sense circuitry is measured, and a waveform is generated based upon the transferred charge. The waveform for one or more cells is analyzed to identify defective cells (i.e., open gate or data line, short to adjacent line, resistive crossing, etc.).

According to the present invention, the gate lines 16 of the array are partitioned into groups (for example, partitioned into groups of 4 gate lines as shown in FIG. 1). A probe pad 21 is provided for each group of gate lines. Gate line select/hold circuitry 17 is integrally formed on the substrate 10 coupled between the probe pad 21 and the group of gate lines, and provides

5 select logic for selectively coupling one or more gate lines for the group to the probe pad 21. Preferably the select logic for the group is controlled by control signals supplied to the select logic via gate select control pads 25 (for example, the 4 gate select control pads 25 shown). Note that for the sake of illustration, the gate select control pads 25 for the second group of gate lines is not shown in FIG. 1. In addition, a second probe pad 27 (not shown in FIG. 1) is preferably

10 provided for the group of gate lines, and the gate line select/hold circuitry 17 for the group includes hold logic for selectively coupling one or more of the gate lines for the group to the second probe pad 27. Preferably the hold logic for the group is controlled by control signals supplied to the hold logic via gate hold control pads 28 (not shown). A more detailed description of the gate line select/hold circuitry 17 and associated control is described below with respect to

15 FIG. 2. Preferably, the second probe pad 27 is shared by more than one group of gate lines.

In addition, the data lines 18 of the array are preferably partitioned into groups (for example, partitioned into groups of 4 data lines as shown in FIG. 1). A probe pad 23 is provided for each group of data lines. Data line select/hold circuitry 19 is integrally formed on the substrate 10 coupled between the probe pad 23 and the group of data lines, and provides select

20 logic for selectively coupling one or more data lines for the group to the probe pad 23. Preferably the select logic for the group is controlled by control signals supplied to the select logic via data select control pads 29 (for example, the 4 data select control pads 29 shown). Note that for the sake of illustration the data select control pads 29 for the second group of data lines is not shown in FIG. 1. In addition, a second probe pad 31 (not shown) is preferably provided for

25 the group of data lines, and the data line select/hold circuitry 19 for the group includes hold logic for selectively coupling one or more of the data lines for the group to the second probe pad 31. Preferably the hold logic for the group is controlled by control signals supplied to the hold logic via data hold control pads 32 (not shown). A more detailed description of the data line

select/hold circuitry 19 is described below with respect to FIG. 3. Preferably, the second probe pad 31 is shared by more than one group of data lines.

Referring to FIG. 2, the gate line select/hold circuitry 17 is coupled between a group of gate lines 16 (for example the 4 gate lines  $GL_0$ ,  $GL_1$ ,  $GL_2$  and  $GL_3$  as shown) and a probe pad 21 for the group. The gate line select/hold circuitry 17 for the group includes select logic 201 that selectively couples one or more gate lines for the group to the probe pad 21 in response control signals supplied via gate select control pads 25. For example, four (4) gate select control pads  $25_0$ ,  $25_1$ ,  $25_2$ ,  $25_3$  may supply four binary control signals to control the select logic 201 for the group as follows:

	Control Signals				Gate Line Coupled to Probe Pad 21 for the Group				Mode
	<u><math>25_0</math></u>	<u><math>25_1</math></u>	<u><math>25_2</math></u>	<u><math>25_3</math></u>	<u><math>GL_0</math></u>	<u><math>GL_1</math></u>	<u><math>GL_2</math></u>	<u><math>GL_3</math></u>	
10	0	0	0	0	N	N	N	N	A and B
15	0	0	0	1	N	N	N	Y	A
	0	0	1	0	N	N	Y	N	
	0	1	0	0	N	Y	N	N	
	1	0	0	0	Y	N	N	N	
20	0	0	1	1	N	N	Y	Y	B
	0	1	0	1	N	Y	N	Y	
	0	1	1	0	N	Y	Y	N	
	0	1	1	1	N	Y	Y	Y	
	1	0	0	1	Y	N	N	Y	
	1	0	1	0	Y	N	Y	N	
	1	0	1	1	Y	N	Y	Y	
	1	1	0	0	Y	Y	N	N	
25	1	1	0	1	Y	Y	N	Y	
	1	1	1	0	Y	Y	Y	N	
	1	1	1	1	Y	Y	Y	Y	

30

Note that the select logic 201 may operate in one of two modes A and B. In mode A, a single gate line is coupled to the probe pad 21 for the group of gate lines. In mode B, more than one gate line is coupled to the probe pad 21 for the group of gate lines. Mode A is preferably used for addressing the cells of the array connected to one gate line of the group. Mode B is

35 preferably used for addressing the cells connected to multiple gate lines of the group.

It should be noted that gate select control pads (for example, the gate select control pads 25<sub>0</sub>, 25<sub>1</sub>, 25<sub>2</sub>, 25<sub>3</sub>) may supply control signals to the select logic 201 for more than one group of gate lines, in which case the addressing function of the select logic 201 for the more than one group of gate lines is replicated. By applying an activation signal to the probe pad 21 for only one group, this configuration may be used to selectively address the cells connected to the gate lines for the one group. Alternatively, an activation signal may be applied to the probe pad 21 for more than one group, thereby addressing multiple cells that are connected to gate lines belonging to different groups. This configuration may be useful in writing charge to and reading charge from multiple cells connecting to gate lines belonging to different groups yet share a common data line.

In addition, a second probe pad 27 is preferably provided for each group of gate lines, and the gate line select/hold circuitry 17 for the group includes hold logic 203 that selectively couples one or more gate lines for the group to the second probe pad 27 in response control signals supplied via gate hold control pads 28. For example, four (4) gate hold control pads 28<sub>0</sub>, 28<sub>1</sub>, 28<sub>2</sub>, 28<sub>3</sub> may supply four binary control signals to control the hold logic 203 for the group as



follows:

Control Signals				Gate Line Coupled to Probe Pad 27 for the Group				Mode
<u>28<sub>0</sub></u>	<u>28<sub>1</sub></u>	<u>28<sub>2</sub></u>	<u>28<sub>3</sub></u>	<u>GL<sub>0</sub></u>	<u>GL<sub>1</sub></u>	<u>GL<sub>2</sub></u>	<u>GL<sub>3</sub></u>	
0	0	0	0	N	N	N	N	A and B
5	0	0	1	N	N	N	Y	A
	0	0	1	0	N	Y	N	
	0	1	0	0	N	Y	N	
	1	0	0	0	Y	N	N	
10	0	0	1	1	N	N	Y	B
	0	1	0	1	N	Y	N	
	0	1	1	0	N	Y	Y	
	0	1	1	1	N	Y	Y	
	1	0	0	1	Y	N	N	
	1	0	1	0	Y	N	Y	
	1	0	1	1	Y	N	Y	
	1	1	0	0	Y	Y	N	
15	1	1	0	1	Y	Y	N	Y
	1	1	1	0	Y	Y	Y	
	1	1	1	1	Y	Y	Y	
20	1	1	1	0	Y	Y	N	Y
	1	1	1	1	Y	Y	Y	

Note that the hold logic 203 may operate in one of two modes A and B. In mode A, a single gate line is coupled to the probe pad 27 for the group of gate lines. In mode B, more than one gate line is coupled to the probe pad 27 for the group of gate lines. Mode A is preferably used for applying a predetermined potential (for example, a test potential as described below in more detail) to a single gate line of the group. Mode B is preferably used for used for applying a predetermined potential (for example, a ground potential as described below in more detail) to multiple gate lines of the group.

It should be noted that gate hold control pads (for example, the gate hold control pads 28<sub>0</sub>, 28<sub>1</sub>, 28<sub>2</sub>, 28<sub>3</sub>) may supply control signals to the hold logic 203 for more than one group of gate lines, in which case the function of the hold logic 203 for the more than one group of gate lines is replicated.

It should be understood by those skilled in the art that when substrate 10 is assembled with a second substrate, spacers, liquid crystal material and a seal, the following components may not be present: the gate line select/hold circuitry 17 for the group, and pads 21, 25, 27 and 28 for the group. In other words, substrate 10 may be cut to remove these elements. In this case,

5 the substrate 10 includes gate line pads that interface to gate line driver circuitry for driving the gates lines of the array during normal operation of the display system. In an alternate embodiment, the probe pad 21, select logic 201 and control pads 25 for the group may interface to the gate line driver circuitry and be integrated into the driving scheme for the array during normal operation.

10 Referring to FIG. 3, the data line select/hold circuitry 19 is coupled between a group of data lines 18 (for example the 4 data lines  $DL_0$ ,  $DL_1$ ,  $DL_2$  and  $DL_3$  as shown) and a probe pad 23 for the group. The data line select/hold circuitry 19 for the group includes select logic 301 that selectively couples one or more of the data lines for the group to the probe pad 23 in response control signals supplied via data select control pads 29. For example, four (4) data select control

15 pads  $29_0$ ,  $29_1$ ,  $29_2$ ,  $29_3$  may supply four binary control signals to control the select logic 301 for

the group as follows:

Control Signals				Data Line Coupled to Probe Pad 23 for the Group				Mode
<u>29<sub>0</sub></u>	<u>29<sub>1</sub></u>	<u>29<sub>2</sub></u>	<u>29<sub>3</sub></u>	<u>DL<sub>0</sub></u>	<u>DL<sub>1</sub></u>	<u>DL<sub>2</sub></u>	<u>DL<sub>3</sub></u>	
0	0	0	0	N	N	N	N	A and B
0	0	0	1	N	N	N	Y	A
0	0	1	0	N	N	Y	N	
0	1	0	0	N	Y	N	N	
1	0	0	0	Y	N	N	N	
0	0	1	1	N	N	Y	Y	B
0	1	0	1	N	Y	N	Y	
0	1	1	0	N	Y	Y	N	
0	1	1	1	N	Y	Y	Y	
1	0	0	1	Y	N	N	Y	
1	0	1	0	Y	N	Y	N	
1	0	1	1	Y	N	Y	Y	
1	1	0	0	Y	Y	N	N	
1	1	0	1	Y	Y	N	Y	
1	1	1	0	Y	Y	Y	N	
1	1	1	1	Y	Y	Y	Y	

Note that the select logic 301 may operate in one of two modes A and B. In mode A, a single data line is coupled to the probe pad 23 for the group of data lines. In mode B, more than one data line is coupled to the probe pad 23 for the group of data lines. Mode A is preferably used for writing charge to (and reading charge from) cells of the array connected to one data line of the group in a single address cycle. Mode B is preferably used for writing charge to (and reading charge from) cells of the array connected to multiple data lines of the group in a single address cycle.

It should be noted that data select control pads (for example, the data select control pads 29<sub>0</sub>, 29<sub>1</sub>, 29<sub>2</sub>, 29<sub>3</sub>) may supply control signals to the select logic 301 for more than one group of data lines, in which case the function of the select logic 301 for the more than one group of data lines is replicated. Charge may be applied to and/or read from a probe pad 23 for only one group of data lines. This configuration may be used to write charge and/or read charge from the cells connected to the data lines for the one group in an address cycle. Alternatively, charge may be

applied to and/or read from the probe pad 23 for more than one group. This configuration may be used to write charge to and/or read charge from multiple cells connected to data lines for more than one group in an address cycle.

It should be noted that mode A of the select logic 301 may be used in conjunction with mode B of the select logic 201 of the gate line select/hold circuitry 17 to write charge to (and read charge from) more than one cell of the array in an address cycle. In addition, mode B of the select logic 301 may be used in conjunction with modes A and B of the select logic 201 of the gate line select/hold circuitry 17 to write charge to (and read charge from) more than one cell of the array in an address cycle. When charge from more than one cell is read from a single data line (Mode A of the select logic 301) or more than one data line (Mode B of the select logic 301), the analysis of the waveform for the cells is adjusted appropriately. In the event that a defect is identified in the cells, the test routine may sequence through the potentially defective cells individually (Mode A of select logic 201 and mode A of select logic 301) to identify the defective cell(s).

In addition, a second probe pad 31 is preferably provided for the group of data lines, and the data line select/hold circuitry 19 for the group includes hold logic 301 that selectively couples one or more data lines for the group to the second probe pad 31 in response control signals supplied via data hold control pads 32. For example, four (4) data hold control pads 32<sub>0</sub>, 32<sub>1</sub>, 32<sub>2</sub>, 32<sub>3</sub> may supply four binary control signals to control the hold logic 303 for the group as

follows:

Control Signals				Data Line Coupled to Probe Pad 31 for the Group					
<u>32<sub>0</sub></u>	<u>32<sub>1</sub></u>	<u>32<sub>2</sub></u>	<u>32<sub>3</sub></u>	<u>DL<sub>0</sub></u>	<u>DL<sub>1</sub></u>	<u>DL<sub>2</sub></u>	<u>DL<sub>3</sub></u>	<u>Mode</u>	
0	0	0	0	N	N	N	N	A and B	
5	<hr/>								
	0	0	0	1	N	N	N	Y	A
	0	0	1	0	N	N	Y	N	
	0	1	0	0	N	Y	N	N	
	1	0	0	0	Y	N	N	N	
10	<hr/>								
	0	0	1	1	N	N	Y	Y	B
	0	1	0	1	N	Y	N	Y	
	0	1	1	0	N	Y	Y	N	
	0	1	1	1	N	Y	Y	Y	
	1	0	0	1	Y	N	N	Y	
	1	0	1	0	Y	N	Y	N	
	1	0	1	1	Y	N	Y	Y	
	1	1	0	0	Y	Y	N	N	
	1	1	0	1	Y	Y	N	Y	
	20	1	1	1	0	Y	Y	Y	
1		1	1	1	Y	Y	Y	Y	

Note that the hold logic 303 may operate in one of two modes A and B. In mode A, a single data line is coupled to the probe pad 31 for the group of data lines. In mode B, more than one data line is coupled to the probe pad 31 for the group of data lines. Mode A is preferably used for applying a predetermined potential (for example, a test potential, as described below in more detail) to a single data lines of the group. Mode B is preferably used for used for applying a predetermined potential (for example, a ground potential, as described below in more detail) to multiple data lines of the group.

It should be noted that data hold control pads (for example, the data hold control pads 32<sub>0</sub>, 32<sub>1</sub>, 32<sub>2</sub>, 32<sub>3</sub>) may supply control signals to the hold logic 303 for more than one group of data lines, in which case the function of the hold logic 303 for the more than one group of data lines is replicated.

It should be understood by those skilled in the art that when substrate 10 is assembled with a second substrate, spacers, liquid crystal material and a seal, the following components may not be present: the data line select/hold circuitry 19 for the group, and pads 23, 29, 31 and 32 for the group. In other words, substrate 10 may be cut to remove these elements. In this case, the substrate 10 includes data line pads that interface to data line driver circuitry for driving the data lines of the array during normal operation of the display system. In an alternate embodiment, the probe pad 23, select logic 301 and control pads 29 for the group may interface to the data line driver circuitry and be integrated into the driving scheme for the array during normal operation.

Importantly, when performing the test routine for the cells of the array, the gate line select/hold circuitry 17 for each group of gate lines is controlled to apply activation signals to the group of gate lines associated therewith and the data line select/hold circuitry 19 for each group of data lines is controlled, such that charge is written and read from the cells of the array via the data lines associated therewith. An example of the control of the gate line select/hold circuitry 17 and data line select/hold circuitry 19 in performing the test routine for the cells of the array is illustrated in FIGS. 4 and 5.

FIGS. 4(A) and (B) illustrate the control of the gate line select/hold circuitry 17 and data line select/hold circuitry 19 in writing charge to a cell connected to an exemplary gate line/data line pair ( $GL_0$ ,  $DL_3$ ) belonging to the group of gate lines and group of data lines illustrated in FIGS. 2 and 3. FIG. 4(A) is a flow chart illustrating the control of the gate line select/hold circuitry 17 and data line select/hold circuitry 19 in writing charge to a cell connected to an exemplary gate line/data line pair ( $GL_0$ ,  $DL_3$ ) in an addressing cycle; and FIG. 4(B) is a timing diagram of an exemplary implementation of the control of FIG. 4(A). Similar operations are performed in writing charge to multiple cells of the array in an address cycle.

Referring to FIG. 4(A), in step 401, probe pad 27 and probe pad 31 are connected to ground potential. In step 403, hold logic 203 of the gate line select/hold circuitry 17 is controlled (via control signals applied to gate hold control pads 28) such that the other gate lines

GL<sub>1</sub>, GL<sub>2</sub>, GL<sub>3</sub> of the group are coupled to ground potential via probe pad 27 and the gate line GL<sub>0</sub> is **not** coupled to the probe pad 27. In step 405, hold logic 303 of the data line select/hold circuitry 19 is controlled (via control signals applied to data hold control pad(s) 32) such that the other data lines DL<sub>0</sub>, DL<sub>1</sub>, DL<sub>2</sub> of the group are coupled to ground potential via probe pad 31 and the data line DL<sub>3</sub> is **not** coupled to the probe pad 31. In step 407, select logic 301 of the data line select/hold circuitry 19 is controlled (via control signals applied to data select control pads 29) such that probe pad 23 is coupled to the data line DL<sub>3</sub> of the cell. In step 409, select logic 201 of the gate line select/hold circuitry 17 is controlled (via control signals applied to gate select control pads 25) such probe pad 21 is coupled to the gate line GL<sub>0</sub> of the cell. In step 411, a charging pulse is applied to the pad 23 (and to data line DL<sub>3</sub> coupled thereto in step 407). In step 413, concurrent with the application of the charging pulse in step 411, an activation pulse is applied to pad 21 (and to gate line GL<sub>0</sub> coupled thereto in step 409). The activation pulse on gate line GL<sub>0</sub> turns the TFT of the cell into a conductive state (ON), thereby providing a conduction path for the charging pulse applied to data line DL<sub>3</sub> to charge the cell.

Note that, in step 403, the hold logic 203 is controlled such that those gate lines not connected to a cell that is to be charged) are coupled to ground potential, and, in step 405, hold logic 303 is controlled such that those data lines not connected to a cell that is to be charged are also coupled to ground potential. These operations ground the inactive gate lines to ground, which minimizes the capacitive coupling between the inactive gate lines and the active (i.e., lines to which the charging pulse is applied) data lines.

FIGS. 5(A) and (B) illustrate the control of the gate line select/hold circuitry 17 and data line select/hold circuitry 19 in reading charge from a cell connected to an exemplary gate line/data line pair (GL<sub>0</sub>, DL<sub>3</sub>) belonging to the group of gate lines and group of data lines illustrated in FIGS. 2 and 3. FIG. 5(A) is a flow chart illustrating the control of the gate line select/hold circuitry 17 and data line select/hold circuitry 19 in reading charge from a cell connected to an exemplary gate line/data line pair (GL<sub>0</sub>, DL<sub>3</sub>) in an address cycle; and FIG. 5(B) is a timing diagram of an exemplary implementation of the control of FIG. 5(A). Similar operations are performed in reading charge from multiple cells of the array in an address cycle.

Referring to FIG. 5(A), in step 501, probe pad 27 and probe pad 31 are connected to ground potential. In step 503, hold logic 203 of the gate line select/hold circuitry 17 is controlled (via control signals applied to gate hold control pads 28) such that the other gate lines  $GL_1, GL_2, GL_3$  of the group are coupled to ground potential via probe pad 27 and the gate line  $GL_0$  is **not** coupled to the probe pad 27. In step 505, hold logic 303 of the data line select/hold circuitry 19 is controlled (via control signals applied to data hold control pad(s) 32) such that such that the other data lines  $DL_0, DL_1, DL_2$  of the group are coupled to ground potential via probe pad 31 and the data line  $DL_3$  is **not** coupled to the probe pad 31. In step 507, select logic 301 of the data line select/hold circuitry 19 is controlled (via control signals applied to data select control pads 29) such that probe pad 23 is coupled to the data line  $DL_3$  of the cell. In step 509, select logic 201 of the gate line select/hold circuitry 17 is controlled (via control signals applied to gate select control pads 25) such probe pad 21 is coupled to the gate line  $GL_0$  of the cell. In step 511, sense circuitry is coupled to the probe pad 23 (and to the data line  $DL_3$  coupled thereto in step 507). In step 513, an activation pulse is applied to pad 21 (and to gate line  $GL_0$  coupled thereto in step 509). The activation pulse on gate line  $GL_0$  turns the TFT of the cell into a conductive state (ON), thereby providing a conduction path for transferring the charge stored in the cell via the data line  $DL_3$  to the sense circuitry coupled thereto in step 511.

Note that in the waveform of FIG. 5(B), the signal denoted "1" illustrates the characteristic signal measured in the event that charge is not stored on the selected cell (i.e., the cell connected to the gate line/data line pair ( $GL_0, DL_3$ )), and the signal denoted "2" illustrates the characteristic signal measured in the event that charge is stored on the selected cell (i.e., the cell connected to the gate line/data line pair ( $GL_0, DL_3$ )).

The test routines described above may identify one (or more) "defective" cells. It may be useful to extend the test routine to determine if the cell is not in fact defective, but a defect exists in the gate line select/hold circuitry 17 and/or in the data line select/hold circuitry 19 associated with the gate line and data line, respectively, connected to the "defective" cell, thereby causing errors in the test routine. For example, an unexpected short circuit or open circuit may exist



between two nodes in the gate line select/hold circuitry 17 and/or the data line select/hold circuitry 19 which cause errors in the test routine.

An open circuit in the gate line select/hold circuitry 17 and/or the data line select/hold circuitry 19 is preferably isolated by performing a continuity test between two suspected open nodes whereby a reference test voltage is applied to one of the suspected open nodes and the voltage at the other suspected open node is read. If the voltages do not match, an open circuit may exist between the two nodes; otherwise, an open circuit does not exist between the two nodes. For example, an unexpected open circuit may exist if the select logic 201 and/or hold logic 203 coupled to the gate lines of the group do not switch properly and remain "open". Such an open circuit may be isolated as follows by performing the following for each gate line in the group: i) control select logic 201 such that the probe pad 21 is electrically coupled to the respective gate line; ii) control hold logic 203 such that probe pad 27 is coupled to the respective gate line; and iii) perform a continuity test to determine if an open circuit exists between the probe pads 21 and 27. If an open circuit exists between the probe pads 21 and 27, an open circuit exists in the select logic 201 and/or hold logic 203 for the gate line of the group. Similar operations may be performed to isolate an open circuit in the select logic 301 and/or hold logic 303 coupled to the data lines of the group.

A short circuit in the gate line select/hold circuitry 17 and/or the data line select/hold circuitry 19 is preferably isolated by applying a reference test voltage to a suspected shorted node, measuring the current at the suspected shorted node while selectively placing each other nodes of the circuit in a high impedance state. If a leakage current disappears when a given node is placed into a high impedance state, the short does not exist between the given node and the suspected shorted node. For example, an unexpected short circuit may exist if the hold logic 203 coupled to the gate lines of the group do not switch properly and remain "closed". Such a short circuit may be isolated as follows by performing the following: i) apply a reference test voltage to probe pad 27 and measure current at probe pad 27; ii) cycle through each gate line in the group and control hold logic 203 such that probe pad 27 is coupled to the respective gate line; and iii) for each gate line, if leakage current disappears, the hold logic 203 is operating properly

for the respective gate line; otherwise, the hold switch for the respective gate line has an unexpected short circuit. Similar operations may be performed to isolate a short circuit in the select logic 201 coupled to the gate lines for the group and to isolate a short circuit in the select logic 301 and/or hold logic 303 coupled to the data lines of the group.

- 5 In the event that a defect is identified in the gate line select/hold circuitry and/or data line select/hold circuitry, the array may be tested manually (or some other test mechanism) to determine if the "defective" cell is in fact defective.

FIG. 1 illustrates an exemplary embodiment of an array tester for performing the test operations of the cells of the array in the manner set forth above. More specifically, the probe pads of the array as described above (probe pads 21,25, 27,28 for each group of gate lines and probe pads 23, 29, 31, and 32 for each group of data lines) are contacted by electrically conductive testing probes extending from a probe fixture 40. A cable 42 has wiring connecting each of the gate line probes (i.e., probes that connect to the probe pads for the groups of gate lines) to gate line drive module 44. A cable 33 has wiring connecting each of the data line probes (i.e., probes that connect to the probe pads for the groups of data lines) to a data line drive/sense module 34. The gate line drive module 44 and data line drive/sense module 34 are controlled by a test controller 46, which executes a control routine that dictates how the test is conducted (such as voltages to be applied, lines to be activated, and analysis of signals read from the cells 12 of the array, the details of which are described above). The test controller 46 interfaces to the gate line drive module 44 via a bus 47, and interfaces to the data line drive/sense module 34 via a bi-directional bus 48. Test controller 46 is connected to a computer system 52 via a bi-directional bus 50. Computer system 52 may be any one of a number of personal computers with suitable software programming support to accomplish the functions described above.

- 25 FIG. 6 illustrates a preferred embodiment of the gate line drive module 44 of FIG. 1. More specifically, the gate line drive module 44 includes gate line drive circuitry 601, multiplexing circuitry 605 and gate line control circuitry 607 that interface to the test controller

46 via bus 47 and interface logic 603. The gate line drive circuitry 601 generates the gate line activation signals under control of the test controller 46. The gate line multiplexing circuitry 605, under control of the test controller 46, selectively switches the gate line activation signals to the probe pads 21 for the groups of gate lines of the array via the cable 42. Finally, the gate line control circuitry 607, under control of the test controller 46, provides the control signals for controlling the gate line select/hold circuitry 17 for the groups of gate lines of the array via cable 42 and the probe pads 25,27,28 associated with each group of gate lines coupled thereto.

Similarly, FIG. 7 illustrates a preferred embodiment of the data line drive/sense module 34 of FIG. 1. More specifically, the data line drive/sense module 34 includes data line drive/sense circuitry 701, multiplexing circuitry 705 and data line control circuitry 707 that interface to the test controller 46 via bus 48 and interface logic 703. The data line drive/sense circuitry 701 includes: drive circuitry that, under control of the test controller 46, generates the charging pulse signals for application to the cells of the array via the data lines; and sense circuitry that, under control of the test controller 46, reads the charge transferred from the cells of the array via the data lines, and generates waveforms based upon the transferred charge. The waveform for one or more cells is analyzed by the test controller 46 to identify defective cells (i.e., open gate or data line, short to adjacent line, resistive crossing, etc.) in the array. A more detailed description of the circuitry and operation of the gate line drive module 44 and the data line drive/sense module 34 may be found in U.S. Patent No. 5,179,345 and 5,546,013, commonly assigned to the assignee of the present invention, herein incorporated by reference in its entirety. The data line multiplexing circuitry 705, under control of the test controller 46, selectively couples the data line drive/sense circuitry 701 to the probe pads 23 for the groups of data lines of the array via the cable 33. Finally, the data line control circuitry 607, under control of the test controller 46, provides the control signals for controlling the data line select/hold circuitry 19 for the groups of data lines of the array via cable 33 and the probe pads 29,31,32 associated with each group of data lines coupled thereto.

Importantly, the present invention provides a flexible interface between the array under test and the test system. More specifically, in the event that the size of the array under test is

changed, the gate line select/hold circuitry 17 and/or the data line select/hold circuitry 19 and the probe pads associated therewith may be designed such that they align with the spacing of an existing probe fixture, thereby eliminating the high costs associated with redesigning the probe fixture for the array. In addition, in the event that the resolution of the array under test is

5 changed, the gate line select/hold circuitry 17 and/or the data line select/hold circuitry 19 and the probe pads associated therewith, along with the appropriate updates to the test routine executed by the array tester, can be used to accommodate for the variations in the number of gate lines and/or data lines, thereby eliminating the costs associated with redesigning the probe fixture for the array.

10 In another aspect of the present invention, the gate line select/hold circuitry 17 for a group of gate lines preferably includes at least one select transistor (which is formed on the substrate 10) and at least one hold transistor (which is formed on the substrate 10) corresponding to each gate line in the group. FIG. 8 illustrates a select transistor/hold transistor pair corresponding to single gate line in a group of gate lines. Note that preferably there would be four (4) select/hold

15 transistor pairs in the gate line select/hold circuitry 17 of FIG. 2. As shown in FIG. 8, the conductive path (channel) of the select transistor 801 is electrically coupled between the probe pad 21 for the group and the corresponding gate line GL of the group, and the control node (gate) of the select transistor 801 is electrically coupled to the gate select control pad 25 for the select transistor. The conductive path (channel) of the hold transistor 803 is electrically coupled

20 between the probe pad 27 for the group and to the corresponding gate line GL of the group, and the control node (gate) of the hold transistor 803 is electrically coupled to the gate hold control pad 28 for the hold transistor 803.

Similarly, the data line select/hold circuitry 19 for a group of data lines preferably includes at least one select transistor (which is formed on the substrate 10) and at least one hold

25 transistor (which is formed on the substrate 10) corresponding data line in the group. FIG. 9 illustrates a select/hold transistor pair corresponding to single data line in a group of data lines. Note that preferably there would be four (4) select transistor/hold transistor pairs in the data line select/hold circuitry 19 of FIG. 3. As shown in FIG. 9, the conductive path (channel) of the

select transistor 901 is electrically coupled between the probe pad 23 for the group and the corresponding data line DL of the group, and the control node (gate) of the select transistor 901 is electrically coupled to the data select control pad 29 for the select transistor. The conductive path (channel) of the hold transistor 903 is electrically coupled between the probe pad 31 for the group and to the corresponding data line DL of the group, and the control node (gate) of the hold transistor 903 is electrically coupled to the data hold control pad 32 for the hold transistor 903.

Because the select transistors and hold transistors of the gate line select/hold circuitry 17 and the data line select/hold circuitry 19 are utilized to transfer charge to/from a capacitive load, the ON resistance of these transistors determines the time constant with which charge is transferred. It is preferable that this time constant, and thus the ON resistance of the transistor be minimized such that the testing time for the cells of the array is minimized. Importantly, the ON resistance of the transistor is proportional to the channel length/width (L/W) ratio of the transistor. Thus, it is preferable that the L/W ratio of these transistor be minimized, which is accomplished by making the channel length (L) of the transistor much greater than the channel width (W) of the transistor ( $L \gg W$ ).

An exemplary layout for a select transistor/hold transistor pair that satisfies these constraints is illustrated in FIGS. 10(A), 10(B) and 10(C). This layout is suitable for use in implementing the select/hold transistor pairs for both the gate line select/hold circuitry 17 and data line select/hold circuitry 19 illustrated in FIGS. 8 and 9.

FIG. 10(A) illustrates the electrodes of the select/hold transistor pair. FIG. 10(B) is a top view illustrating the layout of the select/hold transistor pair of FIG. 10(A). The crosshatching labeled A represents the metal layer for the electrode A of the select transistor, the crosshatching labeled C represents the metal layer for the shared electrode C of the transistor pair, and the crosshatching labeled E represents the metal layer for the electrode E of the hold transistor. A gate electrode B (not shown) for the select transistor is formed above (for a top-gate TFT transistor) or below (for a bottom-gate TFT transistor) a serpentine region between electrodes A and C of the select transistor. This serpentine region represents the channel of the select

transistor. Note that the length  $L$  of the serpentine region (channel) is much larger than its width  $W$  (for example, the length  $L$  may be greater than ten times (10x) the width  $W$  of the channel).

Similarly, a gate electrode  $D$  (not shown) for the hold transistor is formed above (for a top-gate TFT transistor) or below (for a bottom-gate TFT transistor) a serpentine region between

- 5 electrodes  $C$  and  $E$  of the hold transistor. This serpentine region represents the channel of the hold transistor. Note that the length  $L$  of the serpentine region (channel) is much larger than its width  $W$  (for example, the length  $L$  may be greater than ten times (10x) the width  $W$  of the channel).

FIG. 10(C) represents a cross-section A-A' of an exemplary embodiment of the hold transistor of FIG. 10(B) implemented as a bottom-gate TFT transistor. The select transistor of the select/hold transistor pair may be implemented with a similar bottom-gate TFT transistor structure. More specifically, the hold transistor includes a gate electrode layer 951 formed on the substrate 10. The gate metallurgy may utilize a copper or aluminum alloy. An insulating layer 953 (for example, comprising silicon nitride) is formed on the gate electrode layer 951. A layer of amorphous silicon (a-Si) 955 is formed on the insulating layer 953. A patterned insulating layer 957 (for example, comprising silicon nitride) is formed on the a-Si layer 955 to form the channel. A data metal layer 959 is then deposited and patterned to form the  $C$  and  $E$  electrodes of the hold transistor as shown. Finally, a passivation layer (not shown), for example comprising silicon nitride, is formed on resulting TFT structure. An example of the process steps for fabricating such a TFT transistor utilizing a copper gate metallurgy is described in Fryer et al., "A Six Mask TFT/LCD Process Using Copper Gate Metallurgy", IBM Research Report, RC 20594, 1996, herein incorporated by reference in its entirety. An example of the process steps for fabricating such a TFT transistor utilizing an aluminum gate metallurgy is described in Colgan et al., "A 10.5-in.-diagonal SXGA active-matrix display," IBM Journal of Research and Development, Vol. 42, No. 3/4, May/July 1998, pp. 427-444, and in Arai et al., "Aluminum-based gate structure for active-matrix liquid crystal displays," IBM Journal of Research and Development, Vol. 42, No. 3/4, May/July 1998, pp. 491-499, herein incorporated by reference in their entirety. It should be noted that the present invention is not limited to the

layout and structure of the select/hold transistor as illustrated in FIG. 10(C), and thus, any layout/structure may be used to provide the select/hold transistor pair of the present invention.

Importantly, the select and hold transistors of the present invention include a serpentine channel region whereby the length of the serpentine region is much larger than its width  $W$ ,  
5 thereby minimizing the ON resistance of the transistors such that the testing time for the cells of the array is minimized. In addition, the select and hold transistors of the present invention share a common electrode, which minimizes the space (and costs) in integrating the select/hold transistor pair with the array.

While the invention has been described in connection with specific embodiments, it will  
10 be understood that those with skill in the art may develop variations of the disclosed embodiments without departing from the spirit and scope of the following claims.

We claim:

1. In a display system comprising an array of pixel cells formed on a substrate, wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate, a  
5 device comprising:

a first and second transistor formed on said substrate each having a gate electrode and first and second electrodes defining a serpentine channel region there between, whereby voltage applied to said gate electrode controls conductivity of said channel region.

2. The device of claim 1, wherein a common electrode comprises one of said first  
10 and second electrodes of said first transistor and one of said first and second electrodes of said second transistor.

3. The device of claim 1, wherein said first transistor is coupled between a gate line and a probe pad formed on said substrate and selectively couples said probe pad to said gate line during a test routine whereby charge is written to, stored, and read from said array of pixel cells.

4. The device of claim 1, wherein said first transistor is coupled between a data line  
15 and a probe pad formed on said substrate and selectively couples said probe pad to said data line during a test routine whereby charge is written to, stored, and read from said array of pixel cells.

5. The device of claim 1, wherein said second transistor is coupled between a gate  
line and a probe pad formed on said substrate and selectively couples said probe pad to said gate  
20 line during a test routine whereby charge is written to, stored, and read from said array of pixel cells.

6. The device of claim 1, wherein said second transistor is coupled between a data  
line and a probe pad formed on said substrate and selectively couples said probe pad to said data



line during a test routine whereby charge is written to, stored, and read from said array of pixel cells.

## Integrated Circuits for a Display Array

### Abstract of the Disclosure

A device for use in a display system comprising an array of pixel cells formed on a substrate. Each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The device comprises first and second transistors formed on said substrate. Each transistor has a gate electrode and first and second electrodes defining a serpentine channel region there between. Voltage applied to the gate electrode controls conductivity of the channel region. Preferably, the a common electrode comprises one of the first and second electrodes of said first transistor and one of said first and second electrodes of said second transistor. The first and second transistors are preferably coupled between a gate line (or data line) and respective probe pads formed on the substrate and selectively couple the respective probe pad to the gate line (or data line) during a test routine whereby charge is written to, stored, and read from the array of pixel cells.

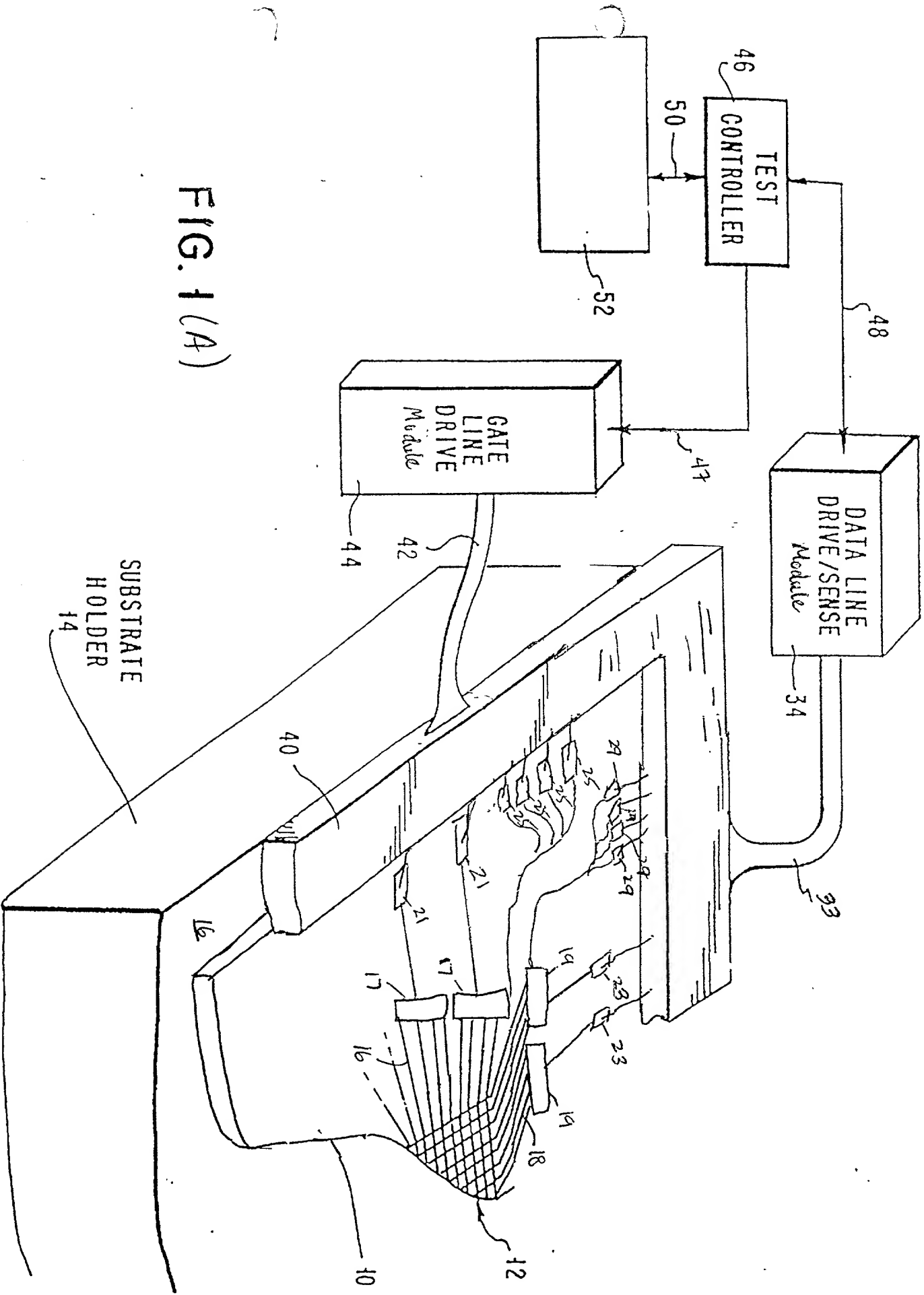


FIG. 1(A)

09009000-040000

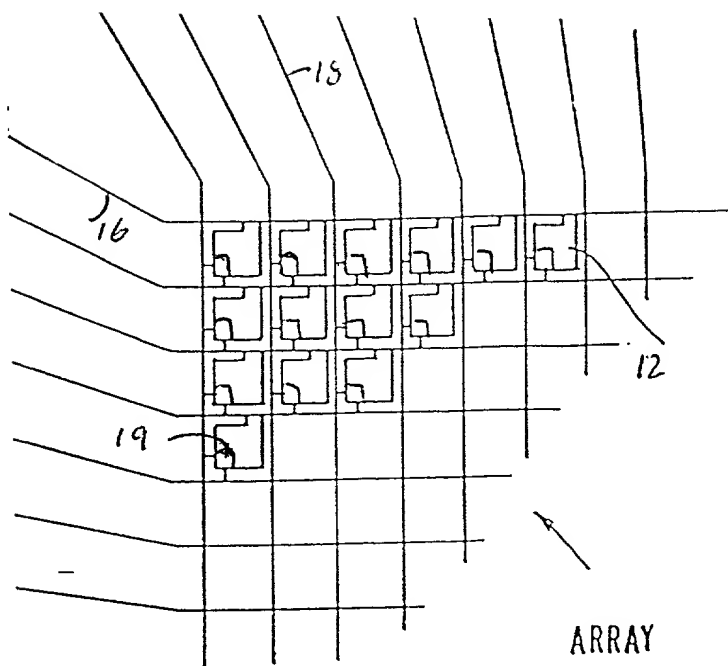


FIG. 1(B)

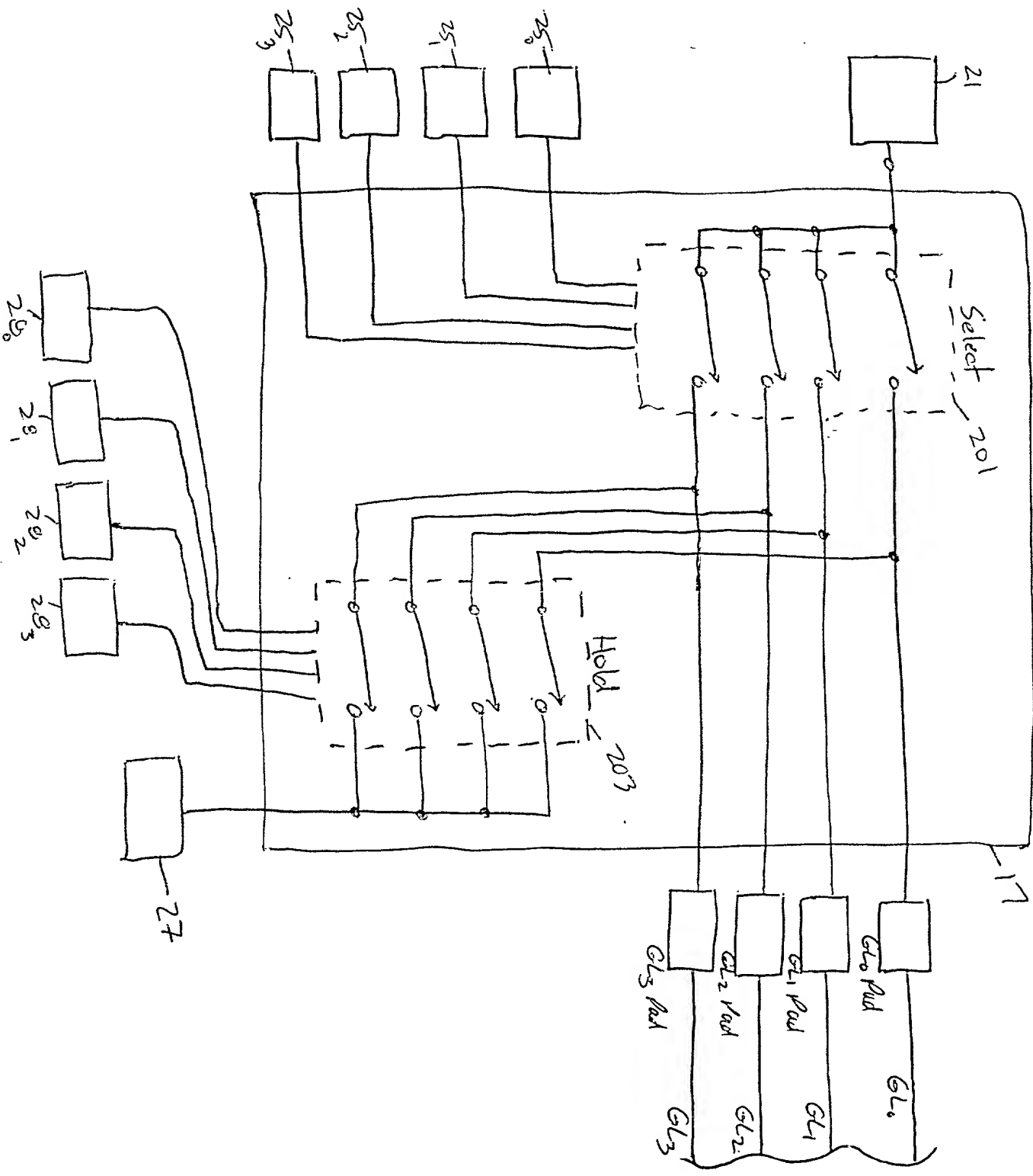


FIG. 2

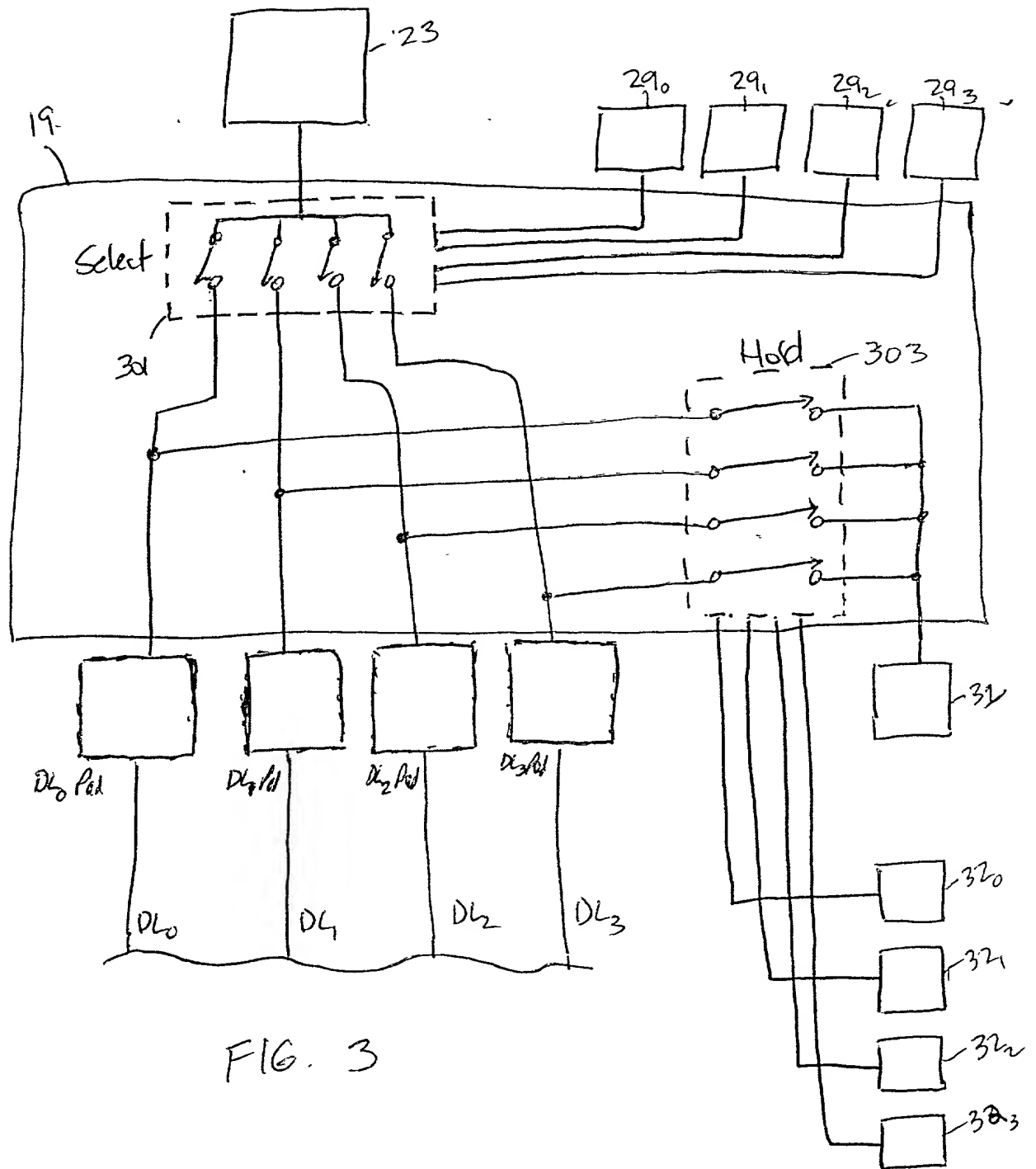
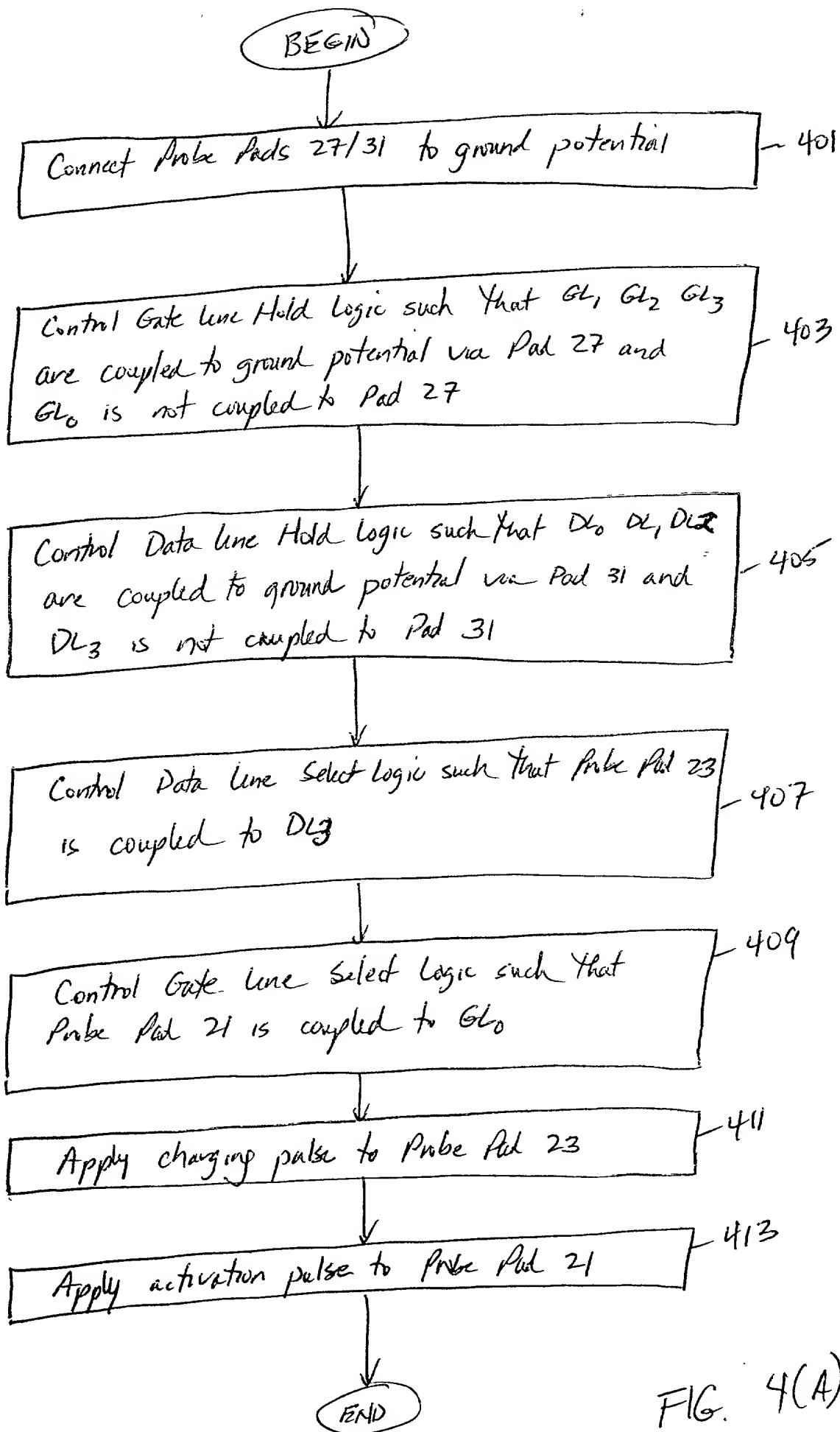


FIG. 3



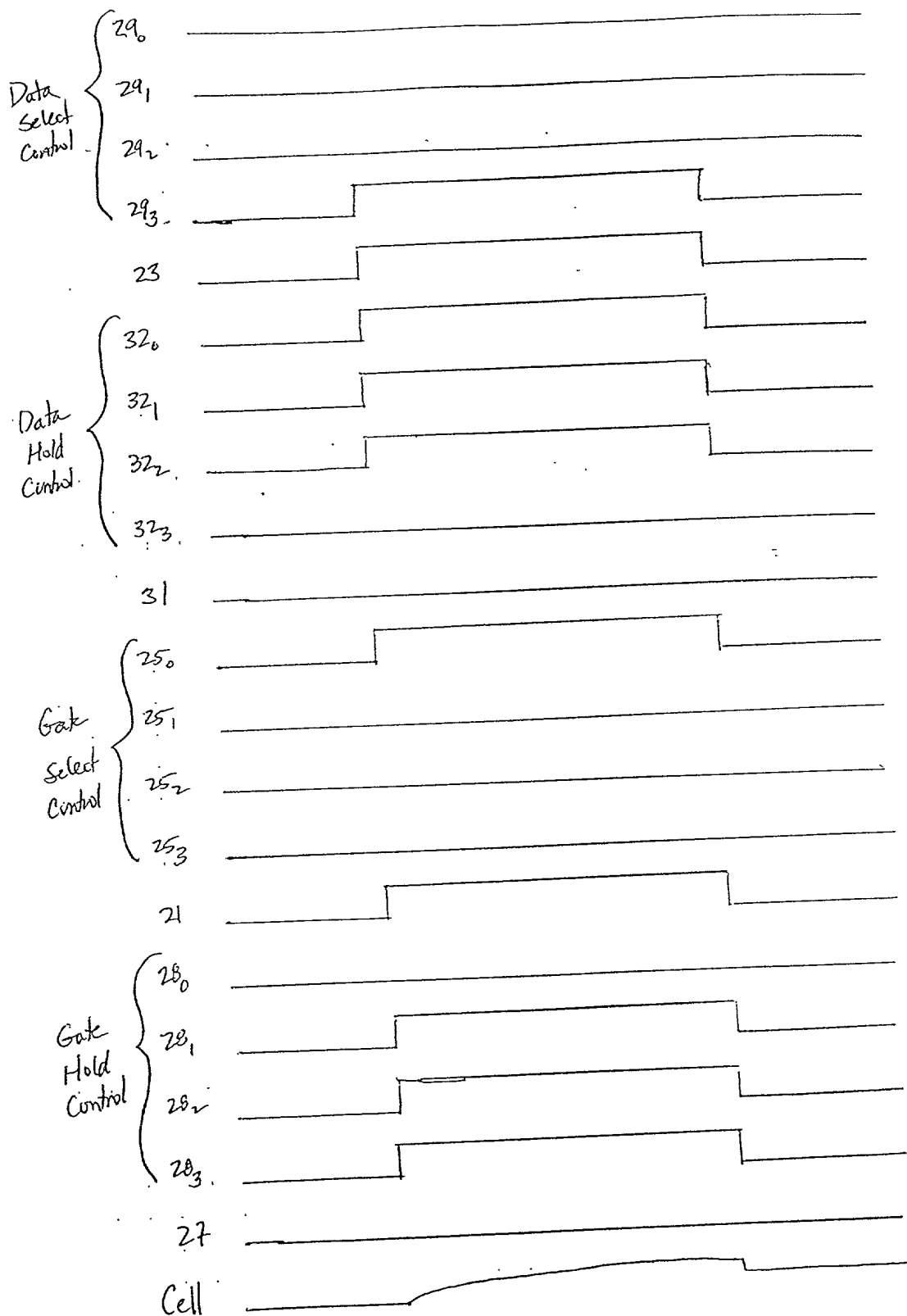


FIG. 4(B)





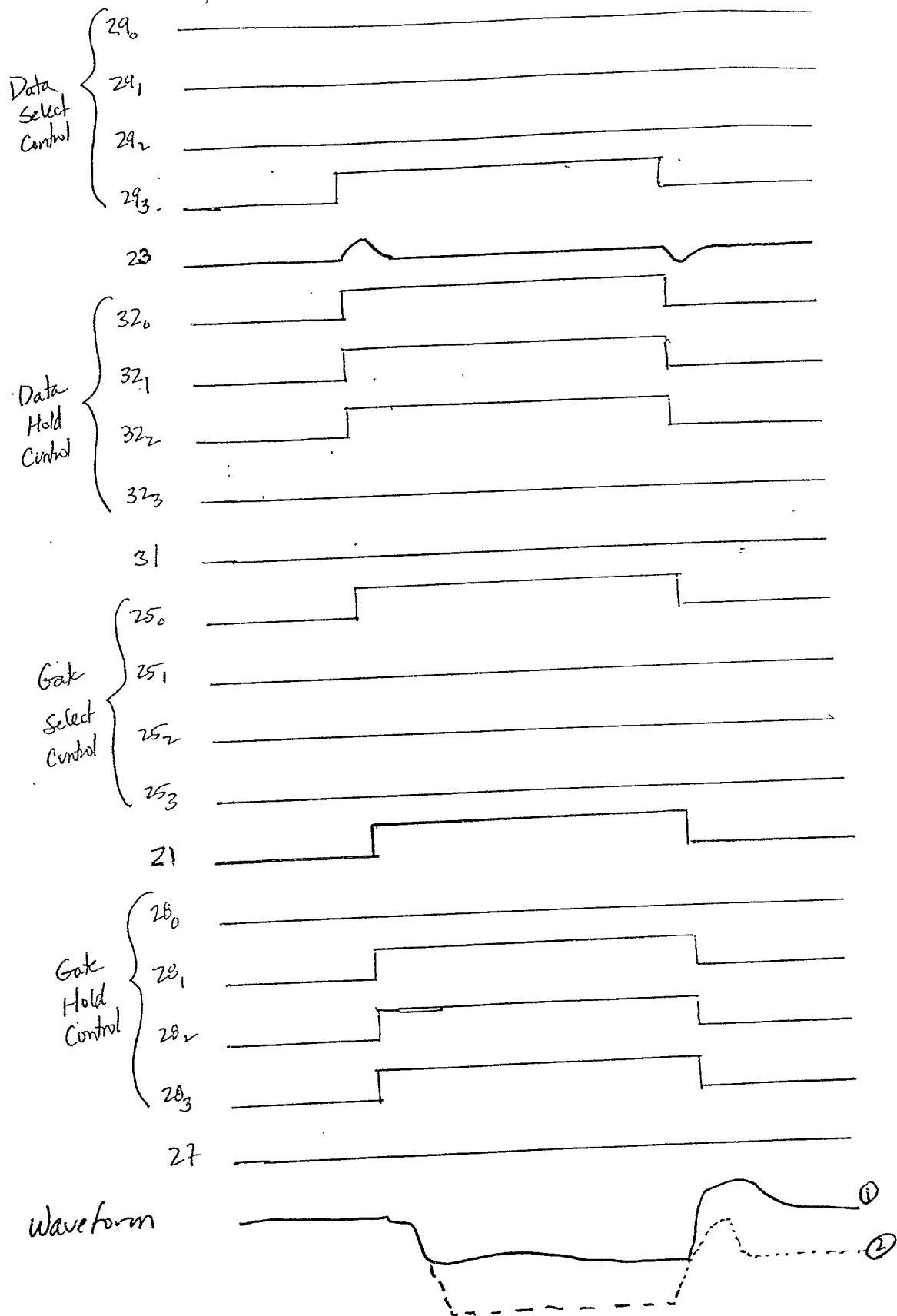


FIG. 5(B)

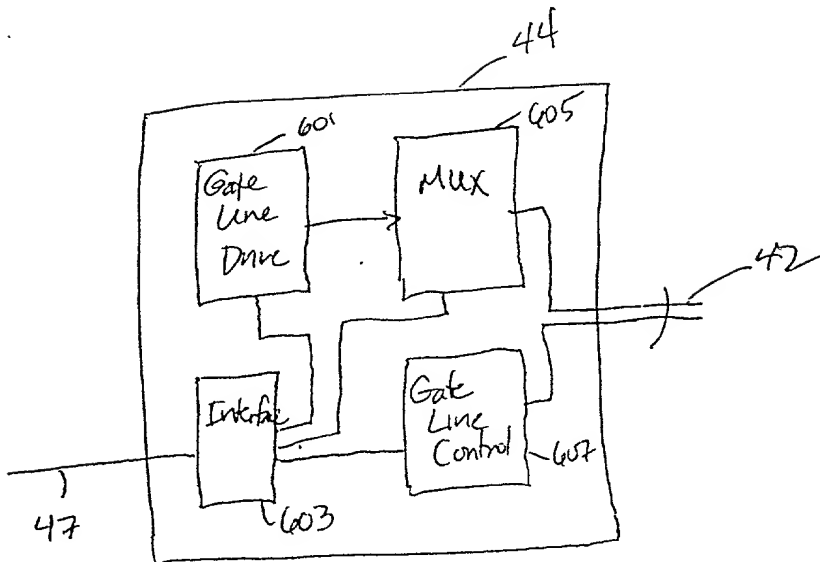


FIG. 6

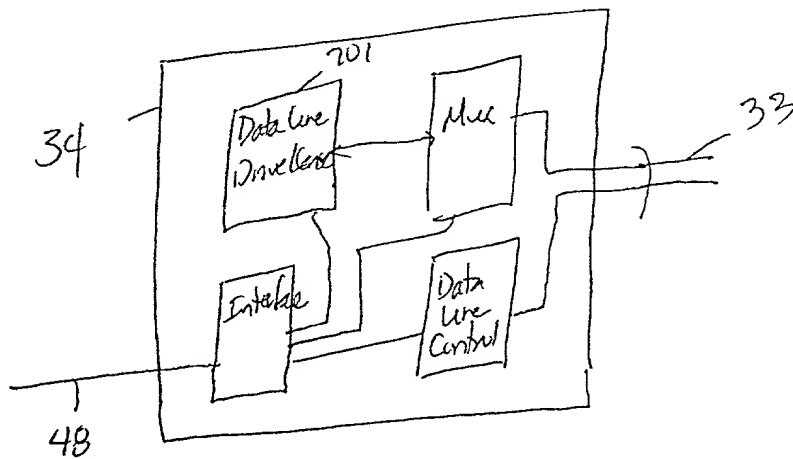


FIG. 7

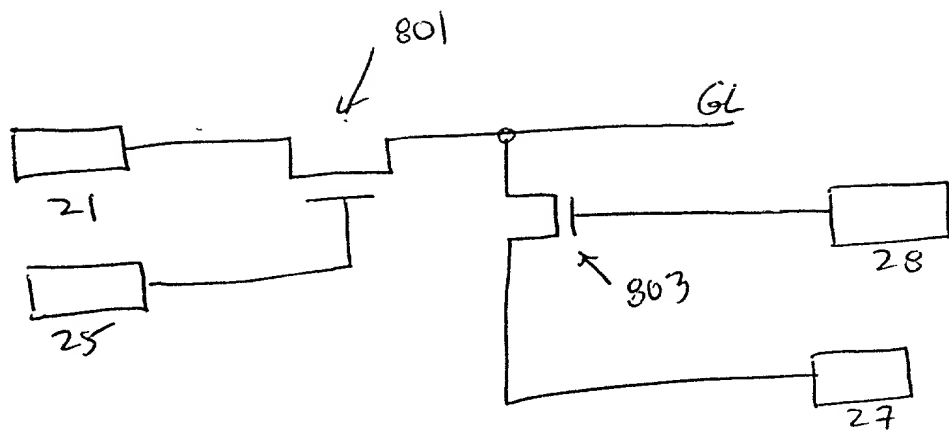


FIG. 8

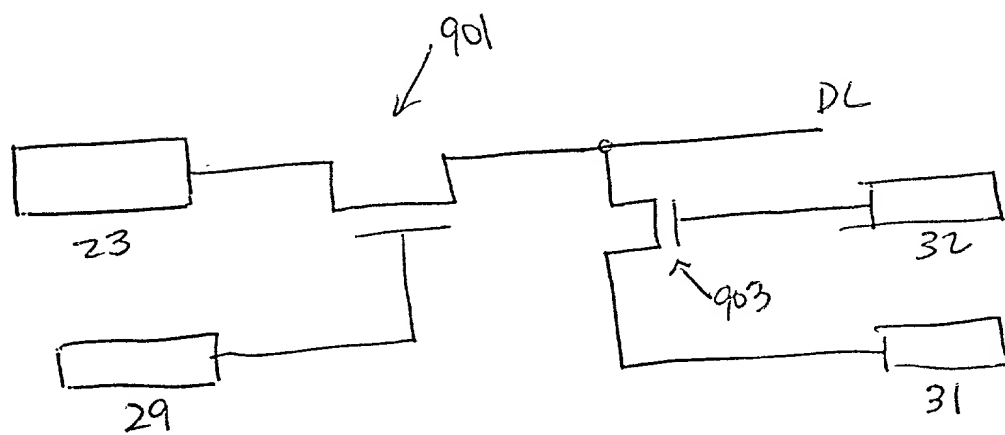


FIG. 9

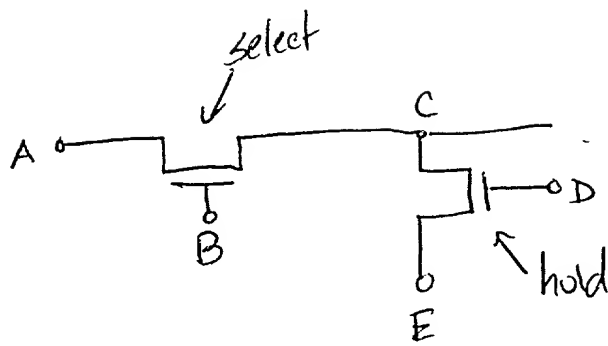


FIG. 10 (A)

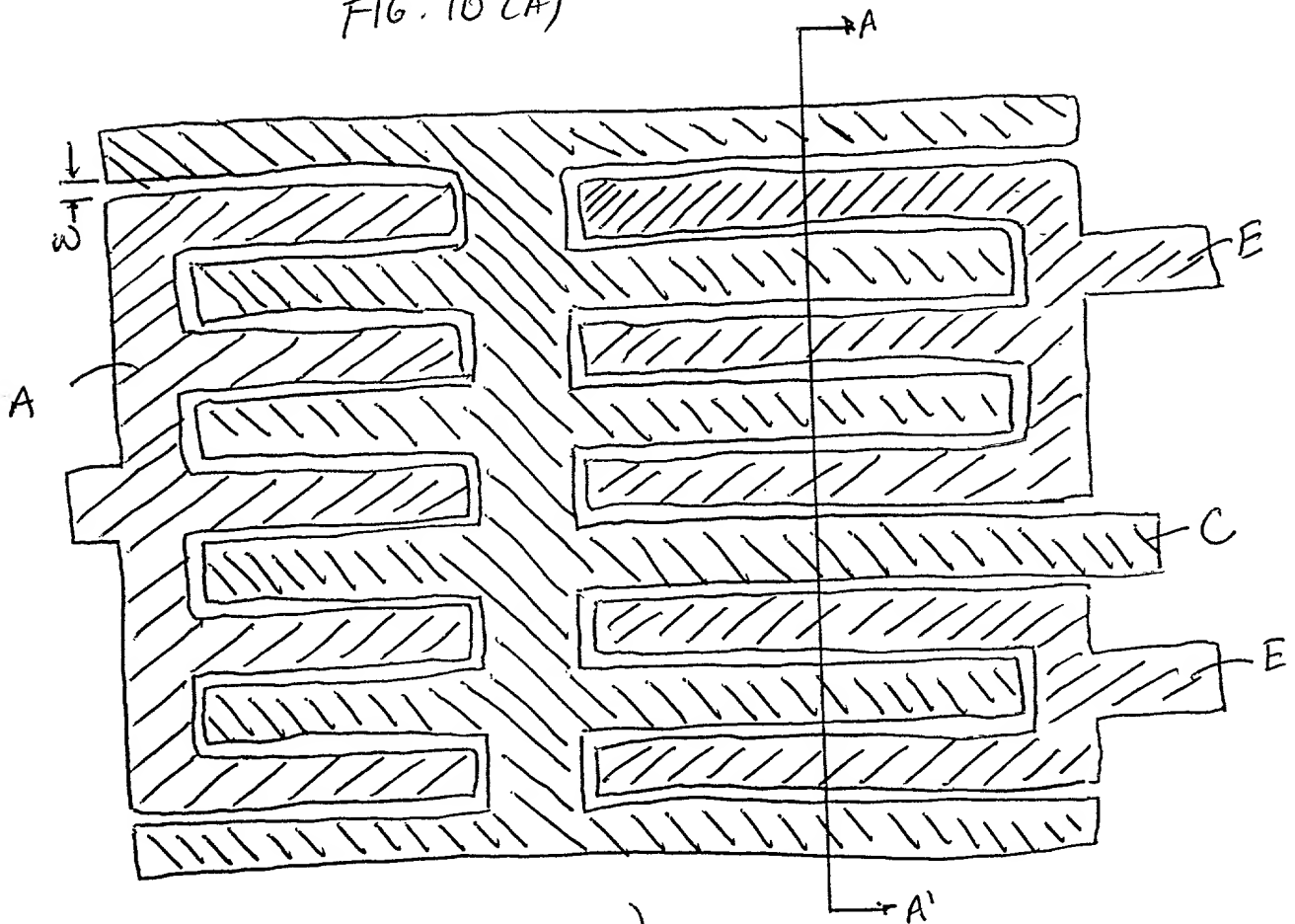


FIG. 10(B)

125b

SSb

1/256

756

959

156

2